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EXAMINER	
VIGUSHIN, JOHN B	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 06/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/739,252	CSONKA ET AL.	
	Examiner	Art Unit	
	John B. Vigushin	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 Apr 2006 & 28 Feb 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-37,40-50 and 52-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *37,40-50 and 52-58* is/are allowed.

6)☒ Claim(s) *12,13,16-20,23-26,29 and 32-36* is/are rejected.

7)☒ Claim(s) *14,15,21,22,27,28,30,31 and 59* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The present Office Action is responsive to Applicant's presently corrected Amendment filed April 11, 2006 and the Remarks from the defective Amendment (due to improper claim presentation) previously filed on February 28, 2006. The Examiner acknowledges the amendments to Claims 37, 40, 41, 49, 59 and the cancellation of Claims 38-39 and 51. Accordingly, Claims 12-36 (withdrawn), 37, 40-50 and 52-59 remain pending in the instant amended Application.

Election/Restrictions

2. The species Restriction Action of April 18, 2005, applied by the previous Examiner, has been reviewed more closely by the present Examiner and found to be unjustified in the opinion of the present Examiner, the Claims 12-36 being merely a broader recitation of the same invention recited in Claims 37, 40-50 and 52-59; not a patentably distinct species. Accordingly, the present Examiner has rejoined Claims 12-36 to the instant Application and has given said rejoined claims an examination on the merits, the results of which are set forth, below.

Claim Objections

3. Claims 25 and 59 are objected under 37 CFR 1.75(a) for the following reasons:

In Claim 25, the next-to-last line, recites "said conducting path" which has no apparent antecedent basis and is mixed with recitations of a "conducting signal path" which may or may not be the same limitation. The objection is to the lack of clarity and

may be overcome by simply changing "conducting path" in line 9 and the next-to-last line of the claim to --conducting signal path--.

In Claim 59, the last line of the claim, recites "said memory controller" for which there is no antecedent basis. This objection may be overcome by changing "said memory controller" to –a memory controller–.

Appropriate correction is required.

Rejections Based On Prior Art

4. The following references were relied upon for the rejections hereinbelow:

Jonaidi (US 6,091,155)† Akram (US 6,008,538)†

Sanwo et al. (US 5,530,623)†

†Already made of record in the previous Office Action of August 31, 2005.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 12, 13 and 16-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Jonaidi.

As to Claim 12, Jonaidi discloses, in Fig. 2, an apparatus of a signal-triggered digital circuit, the apparatus comprising: a signal source for generating a digital signal (col.1: 10-17); an input receiver (IC chip; col.1: 10-17), the input receiver receiving the digital signal for the digital circuit and being responsive to triggering induced by the digital signal (col.1: 10-17); a conducting interface 38; a conducting signal path 40, the conducting signal path 40 being electrically connected to the conducting interface 38, the conducting interface 38 being connected to the input receiver (the input receiver--IC chip--is surface mounted through bump 52 on the conducting interface 38; Figs. 2 and 7 and col.8: 43-47), the signal path 40 carrying the digital signal thereover (col.1: 10-17 and col.5: 29-31); and wherein the conducting interface 38 is substantially rectangular in planar view (Fig. 2 and col.5: 27-29) and the conducting signal path 40 connected thereto as aforesaid has a longitudinal centerline axis which forms an angle in a range of 110 to 160 degrees with respect to a side of conducting interface 38 to which the conducting signal path 40 is connected (Fig. 2 and col.5: 36-38): *Analysis*--i.e., since rectangular conducting interface 38 is approximately 26 mils on each side, then conducting interface 38 is a square, being a special case of the rectangle. Note that in Fig. 2, the center of the square conducting interface 38, its corner and the center of the via 36 are collinear and coincident with the longitudinal centerline axis of conducting signal path 40, distinct from the non-collinear embodiments of Figs.3-5, as pointed out by Jonaidi in col.7: 5-28 (wherein Jonaidi describes the embodiment of Fig. 3 as being distinct from the embodiment of Fig. 2 in that the center of square conducting interface 38, the corner of square conducting interface 38 and the center of via 36 are not

collinear). Now, from geometry it is known that a diagonal of a square includes the center of the square and forms a 45 degree angle with the sides. Accordingly, the supplemental angle formed between the longitudinal centerline axis of conducting signal path 40--which lies coincident with the diagonal of the square pad 38--and the side of the square pad 38 is 135 degrees; i.e., within a range of 110 to 160 degrees. Since the **structure** of the claim has been thusly met by Jonaidi, the **functional limitation** "to thereby produce a reduced reflection of said digital signal at said connection between said conducting interface and said conducting signal path when compared to a connection wherein said angle has a value of 90 degrees" is an inherent property of the connection at an angle of 135 degrees between the conducting interface 38 and the conducting signal path 40 disclosed in the structure of Jonaidi.

As to Claim 13, Jonaidi further discloses the conducting signal path 40 is connected to the conducting interface 38 at a corner thereof (Fig. 2).

As to Claim 16, Jonaidi further discloses the angle in a range of 110 to 160 degrees is an angle of 135 degrees (see *Analysis* in the rejection of Claim 12, above).

As to Claim 17, Jonaidi further discloses a circuit substrate 32, wherein the input receiver and conducting signal path 40 are located on the circuit substrate 32 (Fig. 2; input receiver on circuit substrate 32 is not shown but taught in col.1: 10-25, 29-31 and 37-41; col.5: 14-16).

As to Claim 18, Jonaidi further discloses the circuit substrate 32 comprises a printed circuit board (col.5: 14-16) and wherein conducting interface 38 is a pad and conducting signal path 40 is a trace (Fig. 2 and col.5: 27-31).

As to Claim 19, Jonaidi further discloses pad 38 is substantially square in planar view (Fig. 2 and col.5: 36-38).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jonaidi.

Jonaidi discloses trace 40 has a width of approximately 6 mils (Fig. 2 and col.5: 41-43) and pad 38 has a width of 26 approximately mils (Fig. 2 and col.5: 36-38). So Jonaidi teaches, in Fig. 2, an exemplary land pattern 30 wherein the width of trace 40 is greater than $1/5^{th}$ of a width of pad 38 to which trace 40 is connected (i.e., 6 mil ÷ 26 mil = 0.23 > $1/5^{th}$). However, **Jonaidi further teaches that the exemplary dimensions in**

Fig. 2 can be varied in the disclosed land pattern 30 (col.5: 44-47). Therefore, in order to provide the pad 38 with a size sufficient to accommodate the necessary solder without exhibiting the "pullback" phenomenon, as well as to solve other printed circuit and solder mounting problems disclosed in the Background (cols.1-3), and to accommodate the pitch densities and wire routing layout requirements of a particular circuit board packaging application, it would have been an obvious matter of engineering choice, as suggested by Jonaidi in col.5: 44-47, to optimize the required pad and wiring pitch densities and layout configuration appropriate for each application of the disclosed land pattern 30 of Fig. 2, in accordance with package dimension, cost and other spatial and mechanical packaging process and finished-product requirements for that application. Furthermore, and consistent with the teaching of Jonaidi in col.5: 44-47, and the above-mentioned optimizing of wiring pad and wiring pitch densities, layout configuration, cost and other packaging dimension and spatial and mechanical considerations for the particular application, as suggested in the col.5: 44-47 teaching of Jonaidi, it has been held that discovering an optimum value of a result effective variable [in this case, the trace to pad width ratio of **exactly** $1/5^{th}$ in Claim 20] involves only routine skill in the art. *In re Boesch*, 617 F. 2d 272, 205 USPQ 215 (CCPA 1980).

10. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jonaidi in view of Sanwo et al.

I. Jonaidi discloses control signal sources and input receivers (IC chips) for general purpose use in computers (col.1: 10-17) and does not specify the type of

controller and the type of electronic device within which is located the input receiver (IC chip) and the digital circuit for a specific application.

II. Sanwo et al. discloses a memory device digital circuit (Fig. 2) comprising a memory controller 17 for controlling the input receivers (memory IC chips 43) mounted on cards 31-38 in connectors 21-28 on motherboard 15, the cards 31-38 being memory modules having conducting interfaces for receiving the input receivers (chips 43) and conducting signal paths for carrying the digital signals to and from the memory controller 17.

III. Since Jonaidi discloses control signal sources and IC chips for general purpose use in computers, the use of memory IC chips in a memory device in a computer system and a memory controller to manage the read/write memory functions in the computer system, as taught by Sanwo et al., would have been readily recognized as one of the applications of the land pattern and IC mounting system contemplated in col.1: 10-17 and col.5: 14-16 of Jonaidi.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the controller and input receiver (IC chip) of Jonaidi et al. with the memory controller and memory chip of Sanwo et al. in order to provide a computer system with a memory system, as taught by Sanwo et al., using the effective solder-mounting of the IC chip on the conductive interface taught by Jonaidi, on the memory module of Sanwo et al.

11. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jonaidi in view of Sanwo et al., as applied to Claim 23, above, and further in view of Akram et al.

I. Jonaidi, as modified by Sanwo et al. discloses a circuit substrate (motherboard 15 in Fig. 2 of Sanwo et al.) comprising a slot (connector 21) wherein the memory system further comprises a memory module, say module 31, on which the memory device 43 is located, the memory module 43 being a SIMM (col.1: 18-22; col.6: 6) comprising an edge connector 51 (Fig. 1 and col.3: 15-16), the SIMM being connected to memory controller 17 by edge connector 51 to slot 21 (col.2: 66-col.3: 3).

II. Jonaidi, as modified by Sanwo et al., does not teach the memory module (31 in Sanwo et al.) is a DIMM (dual in-line memory module); rather, memory module 31 is disclosed as a SIMM (single in-line memory module).

III. Akram et al. teaches that SIMM and DIMM devices are known in the art and that, in applications requiring greater memory than can be provided by a SIMM, DIMM devices are used instead (col.1: 31-43).

IV. Therefore, since both Akram et al. and Jonaidi as modified by Sanwo et al., are in a memory device application, then replacing the SIMM 31 of Jonaidi as modified by Sanwo et al. with the DIMM of Akram et al. would have been readily recognized as obvious to one of ordinary skill in the art at the time the invention was made in order to provide and increased memory capability for an application requiring greater memory capacity.

12. Claim 25, 26, 29 and 32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jonaidi.

I. Jonaidi discloses, in Fig. 2, a circuit substrate 32 for a signal-triggered digital circuit, the circuit substrate 32 comprising: a conducting interface 38, substantially rectangular in planar view, for electrical connection to an input receiver (the input receiver--IC chip--is surface mounted through bump 52 on the conducting interface 38; Figs. 2 and 7 and col.8: 43-47), the input receiver receiving a digital signal over the digital circuit (col.1: 10-17) and being responsive to triggering induced by the digital signal (col.1: 10-17); a conducting signal path 40, the conducting signal path 40 being electrically connected to the conducting interface 38, the conducting interface 38 being connected to the input receiver, the signal path 40 carrying the digital signal thereover (col.1: 10-17 and col.5: 29-31); and wherein the conducting interface 38 is substantially rectangular in planar view (Fig. 2 and col.5: 27-29) and the conducting signal path 40 connected thereto as aforesaid has a longitudinal centerline axis which forms an angle in a range of 110 to 160 degrees with respect to a side of conducting interface 38 to which the conducting signal path 40 is connected (Fig. 2 and col.5: 36-38): *Analysis*--i.e., since rectangular conducting interface 38 is approximately 26 mils on each side, then conducting interface 38 is a square, being a special case of the rectangle. Note that in Fig. 2, the center of the square conducting interface 38, its corner and the center of the via 36 are collinear and coincident with the longitudinal centerline axis of conducting signal path 40, distinct from the non-collinear embodiments of Figs.3-5, as pointed out by Jonaidi in col.7: 5-28 (wherein Jonaidi describes the embodiment of Fig.

3 as being distinct from the embodiment of Fig. 2 in that the center of square conducting interface 38, the corner of square conducting interface 38 and the center of via 36 are not collinear). Now, from geometry it is known that a diagonal of a square includes the center of the square and forms a 45 degree angle with the sides. Accordingly, the supplemental angle formed between the longitudinal centerline axis of conducting signal path 40--which lies coincident with the diagonal of the square pad 38--and the side of the square pad 38 is 135 degrees; i.e., within a range of 110 to 160 degrees.

II. Jonaidi discloses that conductive signal path 40 has a width of approximately 6 mils (Fig. 2 and col.5: 41-43) and pad 38 has a width of 26 approximately mils (Fig. 2 and col.5: 36-38). So Jonaidi teaches, in Fig. 2, an exemplary land pattern 30 wherein the width of signal path 40 is greater than $1/5^{th}$ of a width of pad 38 to which signal path 40 is connected (i.e., 6 mil ÷ 26 mil = 0.23 > $1/5^{th}$). However, **Jonaidi further teaches that the exemplary dimensions in Fig. 2 can be varied in the disclosed land pattern 30 (col.5: 44-47)**. Therefore, in order to provide the conducting interface 38 with a size sufficient to accommodate the necessary solder without exhibiting the solder "pullback" phenomenon (col.2: 57-col.3: 18), as well as to solve other printed circuit and solder mounting problems disclosed in the Background (cols.1-3), and to accommodate the pitch densities and wire routing layout requirements of a particular circuit board packaging application, it would have been an obvious matter of engineering choice, as suggested by Jonaidi in col.5: 44-47, to optimize the required pad and wiring pitch densities and layout configuration appropriate for each application of the disclosed land pattern 30 of Fig. 2, in accordance with package dimension, cost and other spatial and

mechanical packaging process and finished-product requirements for that application. Furthermore, and consistent with the teaching of Jonaidi in col.5: 44-47, and the above-mentioned optimizing of wiring pad and wiring pitch densities, layout configuration, cost and other packaging dimension and spatial and mechanical considerations for the particular application, as suggested in the col.5: 44-47 teaching of Jonaidi, it has been held that discovering an optimum value of a result effective variable [in this case, the conducting signal path to conducting interface width ratio of **exactly** $1/5^{th}$ in Claim 25] involves only routine skill in the art. *In re Boesch*, 617 F. 2d 272, 205 USPQ 215 (CCPA 1980).

III. Since the **structure** of the claim has been thusly met by Jonaidi, the **functional limitation** "to thereby produce a reduced reflection of said digital signal at said connection between said conducting interface and said conducting [signal] path when compared to a connection wherein said angle has a value of 90 degrees" is an inherent property of the connection at an angle of 135 degrees between the conducting interface 38 and the conducting signal path 40 disclosed in the structure of Jonaidi.

As to Claim 26, Jonaidi further discloses conductive interface 38 is substantially square in planar view (Fig. 2 and col.5: 36-38).

As to Claim 29, Jonaidi further discloses the conducting signal path 40 is connected to the conducting interface 38 at a corner thereof (Fig. 2).

As to Claim 32, Jonaidi further discloses the angle in a range of 110 to 160 degrees is an angle of 135 degrees (see *Analysis* in the rejection of Claim 25, above).

As to Claim 33, Jonaidi further discloses the circuit substrate 32 comprises a printed circuit board (col.5: 14-16), the conducting interface 38 is a pad and conducting signal path 40 is a trace (Fig. 2 and col.5: 27-31).

As to Claim 34, Jonaidi further discloses circuit substrate 32 further comprises an input receiver (IC chip; col.1: 10-17) and a signal source for generating a digital signal (col.1: 10-17).

13. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jonaidi in view of Sanwo et al.

I. Jonaidi discloses control signal sources and input receivers (IC chips) for general purpose use in computers (col.1: 10-17) and does not specify the type of controller and the type of electronic device within which is located the input receiver (IC chip) and the digital circuit for a specific application.

II. Sanwo et al. discloses a memory device digital circuit (Fig. 2) comprising a memory controller 17 for controlling the input receivers (memory IC chips 43) mounted on cards 31-38 in connectors 21-28 on motherboard 15, the cards 31-38 being memory modules having conducting interfaces for receiving the input receivers (chips 43) and conducting signal paths for carrying the digital signals to and from the memory controller 17.

III. Since Jonaidi discloses control signal sources and IC chips for general purpose use in computers, the use of memory IC chips in a memory device in a computer system and a memory controller to manage the read/write memory functions in the computer system, as taught by Sanwo et al., would have been readily recognized

as one of the applications of the land pattern and IC mounting system contemplated in col.1: 10-17 and col.5: 14-16 of Jonaidi.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the controller and input receiver (IC chip) of Jonaidi et al. with the memory controller and memory chip of Sanwo et al. in order to provide a computer system with a memory system, as taught by Sanwo et al., using the effective solder-mounting of the IC chip on the conductive interface taught by Jonaidi, on the memory module of Sanwo et al.

14. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jonaidi in view of Sanwo et al., as applied to Claim 35, above, and further in view of Akram et al.

I. Jonaidi, as modified by Sanwo et al. discloses a circuit substrate (motherboard 15 in Fig. 2 of Sanwo et al.) comprising a slot (connector 21) wherein the memory system further comprises a memory module, say module 31, on which the memory device 43 is located, the memory module 43 being a SIMM (col.1: 18-22; col.6: 6) comprising an edge connector 51 (Fig. 1 and col.3: 15-16), the SIMM being connected to memory controller 17 by edge connector 51 to slot 21 (col.2: 66-col.3: 3).

II. Jonaidi, as modified by Sanwo et al., does not teach the memory module (31 in Sanwo et al.) is a DIMM (dual in-line memory module); rather, memory module 31 is disclosed as a SIMM (single in-line memory module).

III. Akram et al. teaches that SIMM and DIMM devices are known in the art and that, in applications requiring greater memory than can be provided by a SIMM, DIMM devices are used instead (col.1: 31-43).

IV. Therefore, since both Akram et al. and Jonaidi as modified by Sanwo et al., are in a memory device application, then replacing the SIMM 31 of Jonaidi as modified by Sanwo et al. with the DIMM of Akram et al. would have been readily recognized as obvious to one of ordinary skill in the art at the time the invention was made in order to provide and increased memory capability for an application requiring greater memory capacity.

Allowable Subject Matter

15. Claims 37, 40-50 and 52-58 have been allowed.

16. Claims 14, 15, 21, 22, 27, 28, 30 and 31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

17. Claim 59 is objected to over 37 CFR 1.75(a), as set forth above.

18. The following is an examiner's statement of reasons for allowance:

As to Claims 14-15, patentability resides in the limitation wherein *the conducting signal path has a length which is at least 1/6th of a transition electrical length of the digital signal carried thereover*, in combination with the other limitations of the broadest claim, Claim 14.

As to Claim 21, patentability resides in the limitation wherein *the trace has a thickness which is in a range of 1/5th to 1/6th of a thickness of the pad to which the trace is connected, in combination with the other limitations of the claim.*

As to Claim 22, patentability resides in the exact widths and thicknesses of the pad and trace as recited in the claim, in combination with the other limitations of the claim.

As to Claims 27, patentability resides in the limitation wherein *the conducting signal path has a thickness which is in a range of 1/5th to 1/6th of a thickness of the conducting interface to which the conducting signal path is connected*, in combination with the other limitations of the claim.

As to Claim 28, patentability resides in *the exact widths and thicknesses of the conducting interface and the conducting signal path as recited in the claim*, in combination with the other limitations of the claim.

As to Claims 30-31, patentability resides in the limitation wherein *the conducting signal path has a length which is at least 1/6th of a transition electrical length of the digital signal carried thereover*, in combination with the other limitations of the broadest claim, Claim 30.

As to Claims 37, 40-48, patentability resides in the limitation wherein *the conducting path has a length which is at least 1/6th of a transition electrical length of the digital signal carried thereover*, in combination with the other limitations of base Claim 37.

As to Claims 49, 50 and 52-59, patentability resides in the limitation wherein *the conducting signal path has a thickness which is in a range of 1/5th to 1/6th of a thickness of the conducting interface to which the conducting signal path is connected*, in combination with the other limitations of base Claim 49.

19. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

20. Applicant's arguments, see pp.6-7, filed February 28, 2006, with respect to the Examiner's 35 USC § 112, 2nd paragraph, rejections of Claims 48 and 59 have been fully considered and are persuasive. The Examiner has carefully re-examined and diagrammed the language of dependent Claims 48 and 59 (in conjunction with the language of the intervening and base claims), finding that "said circuit substrate" of dependent Claim 48 is, in fact, the same circuit substrate of Claim 42, from which Claim 48 directly depends, and "said circuit substrate" of dependent Claim 59 is, in fact, the same circuit substrate of Claim 58, from which Claim 59 directly depends. Accordingly, the 35 USC § 112, 2nd paragraph, rejections of Claims 48 and 59 have been withdrawn.

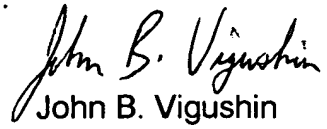
Conclusion

21. Since non-elected Claims 12-36 have been rejoined and given an action on the merits, as set forth above, the present Office Action is made NON-FINAL.

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
June 25, 2006